#11 Appeal Brief D. Smalls-Logan 1-29-03

Docket No.: 57454-257 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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In re Application of	:	
Fukashi MORISHITA	:	
Serial No.: 09/987,566	:	Group Art Unit: 2816
Filed: November 15, 2001	:	Examiner: D. Cunningham

For: INTERNAL POWER SUPPLY VOLTAGE GENERATION CIRCUIT THAT CAN SUPPRESS REDUCTION IN INTERNAL POWER SUPPLY VOLTAGE IN NEIGHBORHOOD OF LOWER LIMIT REGION OF EXTERNAL POWER SUPPLY VOLTAGE

APPEAL BRIEF

Commissioner for Patents
Washington, DC 20231

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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed November 14, 2002.

I. REAL PARTY IN INTEREST

The real party in interest is Mitsubishi Denki Kabushiki Kaisha, the assignee of the entire right, title and interest in and to the above-identified U. S. Application.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known to the Appellant, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

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III. STATUS OF CLAIMS

Claims 19 and 20 are pending. Claims 21 and 22 are cancelled. Claims 19 and 20 stand under final rejection, from which rejection this appeal is taken.

IV. STATUS OF AMENDMENTS

The Advisory Action mailed October 21, 2002 does not indicate the status of the amendment under 37 CFR 1.116 filed on October 8, 2002. However, during a telephone conference of October 29, 2002, Examiner Cunningham advised the Applicant's representative that the Amendment under 37 CFR 1.116 filed on October 8, 2002 will be entered for the purposes of Appeal.

V. SUMMARY OF INVENTION

The present invention relates to an internal voltage generating circuit for generating an internal voltage based on a reference voltage. As shown, for example, in FIG. 1 of the drawings, the internal voltage generating circuit may include a reference voltage generation circuit RG for producing reference voltage Vref that determines a level of internal voltage IntVcc developed by the internal voltage generating circuit supplied with external power supply voltage ExtVcc. In particular, the claimed invention is directed to level detection circuitry, such as lower limit detection circuit 1a shown, for example, in FIGS. 4 and 10 of the drawings. As described on pages 31-36 and 47-52 of the specification and recited in claim 19, the level detection circuitry for detecting a difference between the external power supply voltage ExtVcc and the reference voltage Vref comprises a differential stage including a pair of insulated gate transistors, such as n channel MOS transistors N20 and N21 (FIG. 4)

or N20 and N30 (FIG. 10).

The gate of the insulated gate transistor N20 receives the external power supply voltage ExtVcc, whereas the gate of the transistor N21 or N30 receives the reference voltage Vref. One of the conduction nodes of transistor N20 is connected to one of the conduction nodes of transistor N21 or N30. The second conduction node NDC of transistor N20 is provided for outputting a difference signal corresponding to the difference between the external power supply voltage ExtVcc and the reference voltage Vref.

As shown in FIG. 10 and described on pages 47-48 of the specification, the insulated gate transistor N30 has a current supply ability different from a current supply ability of the insulated gate transistor N20.

As specifically recited in claim 19 and described in the specification in connection, for example, with the structure in FIG. 1, the reference voltage Vref determines a level of the internal voltage IntVcc generated from the external power supply voltage ExtVcc.

The level detection circuitry further comprises operation current supply circuitry for supplying an operation current to the insulated gate transistors N20 and N21 (or N30). This operation current supply circuitry comprises a current mirror, such as a current mirror formed by p-channel transistors P20 and P21, coupled to the transistors N20 and N21 (or N30) for supplying current to these transistors.

In addition, the level detection circuitry comprises a buffer circuit, such as a buffer circuit 1ab (FIGS. 4 and 10), for buffering the difference signal to generate a binary level detection signal indicating whether the external power supply voltage ExtVcc is higher than the reference voltage Vref.

Hence, in accordance with the claimed invention, a power supply voltage is compared with a reference voltage that determines a level of the internal voltage generated based on that power supply

voltage. As a result, a stable internal voltage can be generated over an entire operating range of the power supply voltage, even in a lower region of this range, where a difference between the power supply voltage and the internal voltage becomes smaller and the gain of the internal voltage generating circuit is reduced making it impossible to accurately generate the internal voltage based on comparison between the power supply voltage and the internal voltage.

By comparing the power supply voltage with the reference voltage, the claimed arrangement prevents the internal voltage from becoming excessively low in the lower region of the power supply voltage's operating range.

ISSUES

Whether claims 19 and 20 are anticipated by Bion et al. (5,862,091) under 35 U.S.C. 102(b).

It is noted that in the final rejection, the claims were also rejected under 35 U.S.C. 112, first and second paragraphs. However, the Advisory Action of October 21, 2002 indicates that the amendment under 37 CFR 1.116 of October 8, 2002 overcomes the rejection of the claims under 35 U.S.C. 112.

VI. GROUPING OF CLAIMS

The rejection under 35 U.S.C. 102(b) applied by the Examiner relates to a group composed of claims 19 and 20.

VII. THE ARGUMENT

Rejection under 35 U.S.C. 102(b) is applicable if the publication or issue date of the reference is more than 1 year prior to the effective filing date of the application. However, the effective filing date of the present application is September 8, 1998, which is before the issue date of the Bion patent (January 19, 1999). It is noted that in the preliminary Amendment of November 15, 2001, the present application was amended to recite that this application is a continuation of U.S. Application Serial No. 09/739,227, filed December 19, 2000, which is a continuation of U.S. Application Serial No. 09/149,079, filed September 8, 1998, now U.S. Patent No. 6,184,744.

Hence, the Bion et al. patent is not a reference under 35 U.S.C. 102(b).

Further, anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989). The term "anticipation," in the sense of 35 U.S.C. 102, has acquired the accepted definition meaning "the disclosure in the prior art of a thing substantially identical with the claimed invention." ***In re Schaumann***, 572 F.2d 312, 197 USPQ 5 (CCPA 1978). The initial burden of establishing a basis for denying patentability to a claimed invention rests upon the Examiner. ***In re Fine***, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***In re Thorpe,*** 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985); ***In re Piasecki,*** 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984). To satisfy this burden, therefore, each and every element of the claimed invention must be shown by the Examiner to be disclosed in Bion et al. To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by

persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Appellant respectfully asserts that the record fails to meet this requirement.

Independent claim 19 recites level detection circuitry for detecting a difference between a first voltage and a second voltage. The circuitry comprises a differential stage including a first insulated gate transistor and a second insulated gate transistor. The first insulated gate transistor receives a power supply voltage as the first voltage at a gate thereof and has a first conduction node, and a second conduction node for outputting a difference signal. The second insulated gate transistor receives a reference voltage as the second voltage at a gate thereof and having a first conduction node connected to the first conduction node of the first insulated gate transistor. The second insulated gate transistor has a current supply ability different from a current supply ability of the first insulated gate transistor under a condition of the same gate voltage. The difference signal corresponds to a difference between the first and second voltages. The reference voltage determines a voltage level of an internal voltage generated from the power supply voltage.

Also, the level detection circuitry comprises:

-operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors, the operation current supply circuitry comprising a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors; and

-a buffer circuit for buffering the difference signal for generating a binary level detection signal indicating whether the first voltage is higher than the second voltage.

In the Advisory Action of October 21, 2002, the Examiner takes the position that the inverting input of amplifier 37 (FIG. 11 of Bion et al.) corresponds to the gate of the "first transistor" and is

connected to a "power supply voltage" Vcc by way of transistor 36, and the non-inverting input of 37 corresponds to the gate of the "second transistors" and is connected to a "reference voltage" which is the internal voltage generated from said power supply Vcc by way of resistor-connected transistor 38.

Considering the reference, FIG. 11 of Bion et al. shows a read circuit 35 having p blocks 34. The outputs of the blocks 34 are connected to the drain of a precharging transistor 36, which is coupled to the inverting input of a differential amplifier 37. The inverting input of this transistor is connected to the drain of a reference transistor 38 which is identical to the precharging transistor 38. The source of the reference transistor 38 is connected to the supply voltage Vcc, and its gate is grounded so as to always maintain transistor 38 in an on condition.

The output of the comparator 37 corresponds to the output of the read circuit 35. The comparator 37 receives a voltage through transistor 38 at its non-inverting input, in order to compensate for the voltage drop via the precharging transistor 36 at the data read out node (corresponding to the inverting input).

Hence, the output of the comparator 37 does not produce a difference signal corresponding to a difference between the power supply voltage Vcc and the reference voltage produced from the power supply voltage Vcc. Instead, the output of 37 produces the read out data supplied to the inverting input. The voltage drop at the precharging transistor 36 (at the inverting input) is compensated by the voltage drop at the identical reference transistor 38 (at the non-inverting input). Moreover, it is noted that the transistor 38 is employed to compensate for the voltage drop at the precharging transistor 36 that precharges the inverting input, which is not precharged to a power supply voltage level.

Accordingly, the reference does not disclose the claimed differential stage producing a difference signal corresponding to a difference between a power supply voltage and a reference voltage that determines a voltage level of an internal voltage generated from the power supply voltage, as claim

19 requires.

Further, the transistor 38 is employed for compensating for the voltage drop at the precharging transistor 36 to maintain the voltages at non-inverting and inverting input nodes of the comparator at the same voltage level in the standby state. Then, a memory cell is selected, and the comparator determines whether the precharge node is discharged by the comparator, and memory cell data is read out in accordance with the result of this determination.

Therefore, if the reference voltage at the non-inverting input corresponded to the internal voltage, as the Examiner contends, then the both inputs of the comparator 37 would receive the same internal voltage, and the comparison with the power supply voltage would not be performed. 2

Further, as discussed above, Bion et al. does not disclose a detection signal indicating whether the power supply voltage is higher than the reference voltage that determines the internal voltage generated from the power supply voltage.

Therefore, Bion et al. cannot disclose the claimed buffer circuit for buffering the difference signal for generating a binary level detection signal indicating whether the first voltage is higher than the second voltage. 3

Accordingly, it is respectfully submitted that Bion et al. does not anticipate the invention recited in claim 19 within the meaning of 35 U.S.C. 102.

Claim 20 dependent from claim 19 is defined over the reference at least for the reasons presented above in connection with claim 19.

VIII. CONCLUSION

For the reasons advanced above, Appellant respectfully contends that the rejection of claims 19 and 20 as being anticipated under 35 U.S.C. § 102 is improper as the Examiner has not met the burden of establishing a *prima facie* case of anticipation. Reversal of the rejection in this appeal is respectfully requested.

Respectfully submitted,

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IX. APPENDIX

19. Level detection circuitry for detecting a difference between a first voltage and a second voltage, comprising:

a differential stage including a first insulated gate transistor and a second insulated gate transistor,

said first insulated gate transistor receiving a power supply voltage as the first voltage at a gate thereof and having a first conduction node, and a second conduction node for outputting a difference signal, and

said second insulated gate transistor receiving a reference voltage as the second voltage at a gate thereof and having a first conduction node connected to said first conduction node of said first insulated gate transistor, said second insulated gate transistor having a current supply ability different from a current supply ability of said first insulated gate transistor under a condition of the same gate voltage, and said difference signal corresponding to a difference between the first and second voltages, said reference voltage determining a voltage level of an internal voltage generated from said power supply voltage;

operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors, said operation current supply circuitry comprising a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors; and

a buffer circuit for buffering said difference signal for generating a binary level detection signal indicating whether said first voltage is higher than said second voltage.

20. The level detection circuitry according to claim 19, wherein said first insulated gate transistor is smaller in channel width than said second insulated gate transistor.